POWER SUPPLY SEQUENCING

For proper operation DV_{DD} should be applied first and AV_{DD} simultaneously or within 10ms of DV_{DD}. This ensures that the power on reset circuitry sets the registers to their default values and keep the analog outputs at 0 V until a valid write operation takes place. When AV_{DD} cannot be applied within 10ms of DV_{DD} a hardware reset should be issued. This will trigger the power on reset circuitry and load the default register values. For cases where the power supply applied first has the same or lower voltage than the second supply a schottkey diode can be used to supply power until the second power supply turns on. Table 18 lists power supply sequences and the recommended diode connection. Alternatively, a load switch such as the ADP196 can be used to delay the first power supply until the second power supply turns on. Figure 32 shows a typical configuration using the ADP196. In this case the AVDD is applied first. This voltage does not appear at the AVDD pin of the AD5380 until the DVDD is applied and brings the EN pin high. The result is that the AVDD and DVDD are both applied to the AD5380 at the same time.

Table 18. Power Supply Sequencing

First Power Supply	Second Power Supply	Recommended Operation
AV_{DD} = 3 V	DV_{DD} ≥ 3 V	See Figure 30.
DV_{DD} = 3 V	AV_{DD} ≥ 3 V	See Figure 31.
AV_{DD} = DV_{DD}	DV_{DD} = AV_{DD}	See See Figure 30; assumes separate analog and digital supplies.
DV_{DD} = AV_{DD}	AV_{DD} = DV_{DD}	See Figure 31; assumes separate analog and digital supplies
AV_{DD} = 5 V	DV_{DD} = 3 V	See Figure 32
DV_{DD} = 5 V	AV_{DD} = 3 V	Hardware reset or see Figure 33

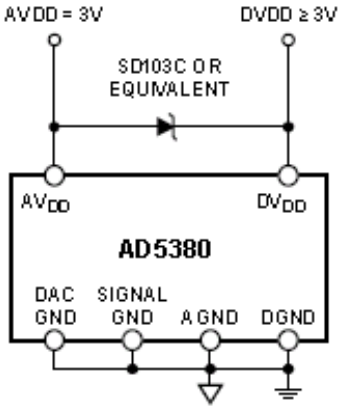

Figure 30. AVDD first followed by DVDD

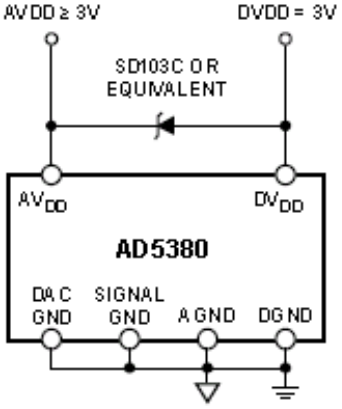

Figure 31. DVDD first followed by AVDD

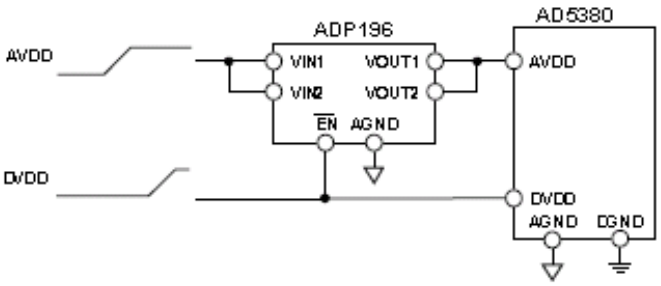

Figure 32. AVDD Power supply controlled by a load switch

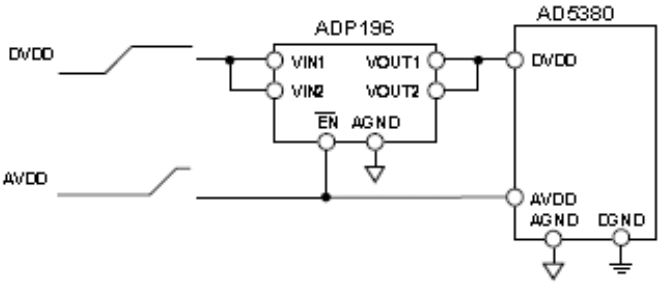

Figure 33. DVDD Power supply controlled by a load switch

s

Interface Timing corrections

Parameter	Current Data Sheet Specification	Corrected Data Sheet Specification	Unit	Description
t_{7A}	50	140	ns min	Minimum $\overline{\text{SYNC}}$ high time in Readback mode
t_{10}	30	36	ns max	24th SCLK falling edge to $\overline{\text{BUSY}}$ falling edge
t_{14}	2000 max	100/2000	ns min/max	$\overline{\text{BUSY}}$ rising edge to DAC output response time
t_{17}	8	3	µs typ	DAC output settling time; boost mode off
t_{20}	20	30	ns max	SCLK rising edge to SDO valid